

# Switching: Performance and Architecture Issues

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# Outline

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- Performance measures
- Architectural issues

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# Introduction

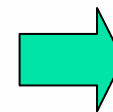
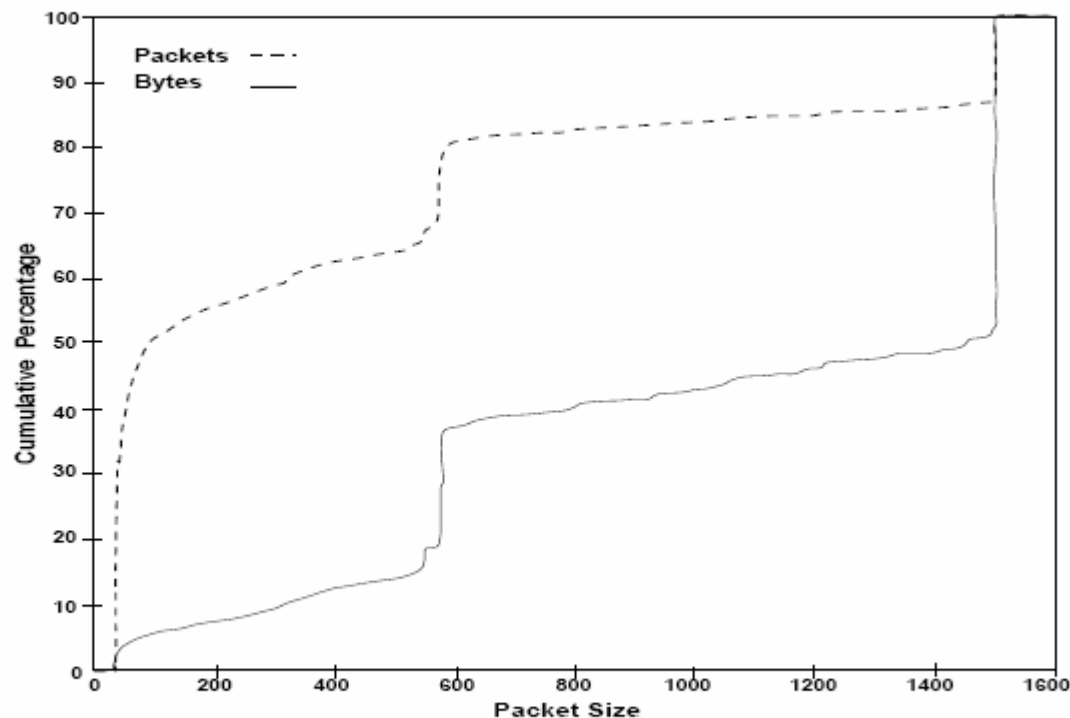
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- Transmission capacity is expensive; Switching helps in improving efficiency of transmission capacity usage by enabling a greater degree of multiplexing.
- This in turn is achieved by enabling an information flow to traverse multiple links by moving (switching) flows among the links that are interconnected through the switch.
- Two basic kinds of switches – Circuit and Packet
- Links interconnects by switches could be asynchronous (like Ethernet) or synchronous (like ATM).

# Packet processing capacity

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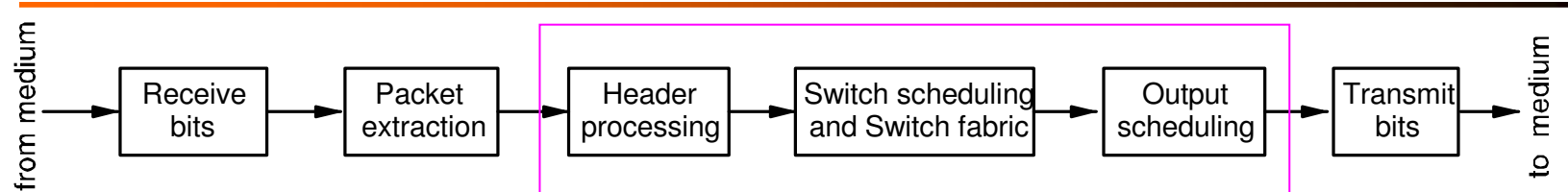
- Processing time per packet is independent of the length
- Sample cumulative packet length distribution (from NASA AIX)



Small packets dominate, thus the packet-processing rate of a switch should be dimensioned with this in mind.

Dotted: fraction of packets with length less than  $x$  bytes  
Solid: fraction of bytes in packets with size less than  $x$  bytes.

# Passage of a packet through a switch



- Header processing: route lookup and packet classification
  - Header processing time should be constant to ensure QoS (e.g., delay)
    - Variability in processing time can cause packet queue to build up at the input, and a packet will experience variable delay before its service category is determined
- Switch queueing is necessary to resolve output contention
- Switch could “block”, and blocking probability should be minimized

## Passage of a packet (contd.)

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- Switch design objective
  - QoS for stream sessions is achieved by scheduling on output link
  - To provide QoS, packets should reach output queue with constant latency, or packets should be available for output scheduling with constant latency

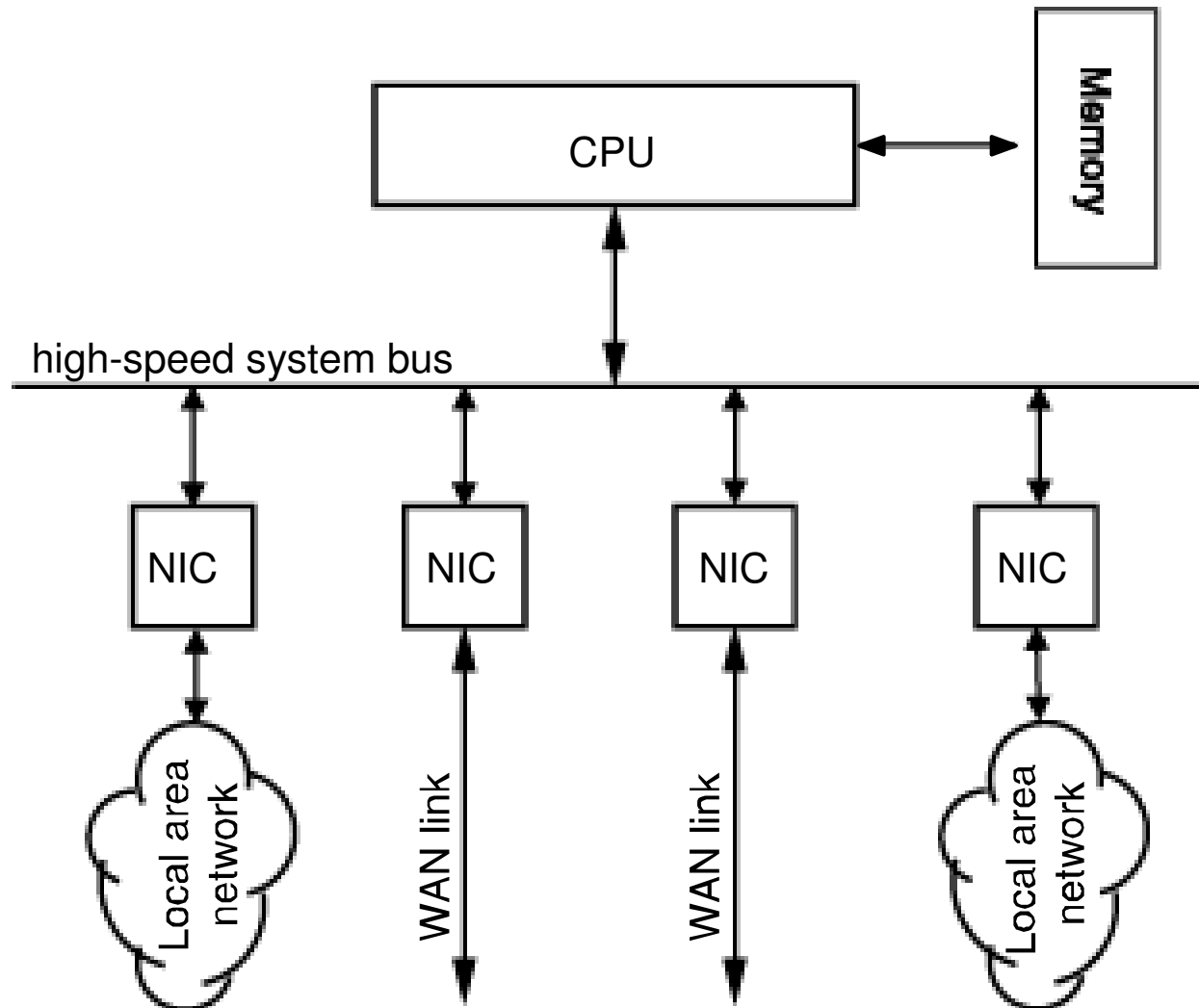
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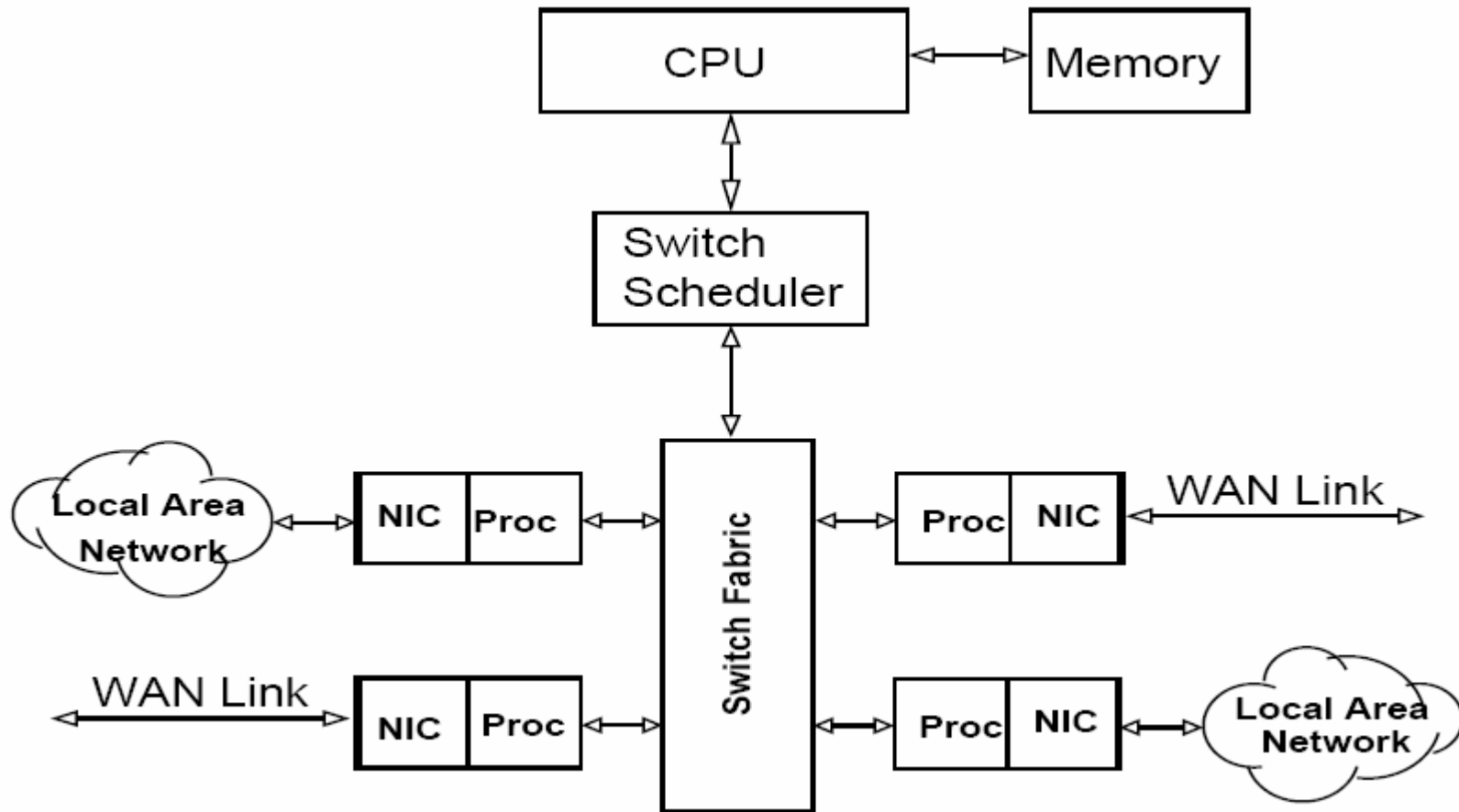
# Switches based on general-purpose CPU and NICs

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# Fabric based switches

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# Fabric based switches (contd.)

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- A space switching fabric creates physical path between the input and output ports and it can create such paths between many input-output pairs simultaneously.
- Immediate design issue: Rate at which packets may be switched relative to line rates.
- Assume a time slotted switch; In a slot, let  $p$  be the maximum number of packets that can be switched from an input, and let  $q$  be the maximum number of packets that it can switch to an output.
- If  $p = 1$  and  $q = 1$ , we have an *input queued (IQ)* switch;  $p = 1$  and  $q = N$  corresponds to the *output queued (OQ)* switch. # of input or output ports
- If  $p < N$ , a packet queue should be maintained at the input and if  $q > 1$  a packet queue should be maintained at the output. Thus  $p < N$  and  $q > 1$  yields in an a *combined input output queued switch (CIOQ)*.
- $p, q > 1$  is achieved by a *speedup* of the fabric or by *parallelism*.  
Fabric operating rate > link rate Fabric simultaneously selecting more than one packet from an input or to an output

- Chapter 10: queueing in packet switches
- Chapter 11: switching fabrics
- Chapter 12: packet processing